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2012 Definitions for EDA Market Share Survey

The first page of the attached survey form is a summary page of all your company's EDA software activities. Subsequent pages further divide your software and software maintenance revenue by sub-application detail.

REVENUE, requested in U.S. $ million, is for those products sold into the EDA market:

A. **TOTAL REVENUE** is the sum of B, C, and D below.
B. **SOFTWARE REVENUE** is revenue from the sale of applications software.
C. **SOFTWARE MAINTENANCE REVENUE** is fees for software maintenance.
D. **OTHER SERVICE REVENUE** is revenue derived from the service and support of technical software systems. It includes the following:

1. **Hardware Maintenance** - fees for hardware maintenance
2. **Consulting Revenue** - assessment of technical software business and information technology (IT) needs and the formulation of a plan based on needs identification
3. **Management and Operations Services** education and training, help desk, disaster recovery, vaulting, facilities management, configuration management
4. **Service Bureau** - construction of database, data conversion, product design, analysis, or manufacturing
5. **Application Development** - design and development of customized software applications; modification, enhancement or customization of existing software applications, adding new functionality
6. **Implementation and Integration Services** - planning, implementation, migration, and integration of software products (software network support and integration, account integration management, data center design and construction).

REGIONAL REVENUE DISTRIBUTION:
Please indicate revenue distribution by world regions:

North America includes the United States and Canada

Europe includes Austria/Switzerland, Belgium/Netherlands/Luxembourg, Central Europe (Belarus, Bulgaria, Czech Republic, Estonia, Hungary, Latvia, Lithuania, Poland, Russia, Slovakia and Ukraine), France, Germany, Italy, Russia, Scandinavia (Denmark, Finland, Norway and Sweden), Spain, United Kingdom, and Rest of Europe

Japan is a single-country region

Asia/Pacific includes Australia, China, Hong Kong, India, South Korea, Singapore, Taiwan and Rest of Asia

Rest of World includes Latin America and Middle East/Africa

APPLICATION REVENUE BREAKDOWN:
Please indicate your revenue splits by application according to the following definitions

Electronic Design Automation covers computer-based tools to automate the design of electronic products divided into:

Electronic CAE (Electronic computer-aided Engineering) are tools used in the engineering or design phase (as opposed to the physical layout phase of the product) of electronic products

IC Layout tools are used to create and validate the physical implementation of an integrated circuit (IC), including polygon editors, symbolic editors, placement and routing

PCB (Printed Circuit Board) Layout/Hybrid/MCM (Multichip Module) tools are used to create the placement and routing of traces and components on a PCB

ECAE SUB-APPLICATION DEFINITIONS

ELECTRONIC SYSTEM LEVEL (ESL)

ELECTRONIC SYSTEM LEVEL
Concurrent design of hardware and software

BEHAVIORAL LEVEL
ESL design prior to hardware/ software partitioning

- **Architect's Workbench** – A virtualization platform used to develop the products specification

ARCHITECTURAL LEVEL
ESL design after hardware/software partitioning

ESL HARDWARE DESIGN
- **ESL Design and Entry** - Tools designed to assist engineers in entering a design or analyzing the simulated results of that design at the Transactional Level
- **ESL Simulation** - Simulation at the Transaction Level
- **ESL Synthesis -** Synthesis at the Transactional Level
- **HLD Synthesis (High Level Design) or ESL Synthesis -** Synthesis at the Transactional Level
- **ESL Power Analysis -** Analyzing Power optimization at the Transactional Level
- **ESL Thermal Analysis -** Analyzing heat distribution at the Transactional Level
- **ESL Target Compiler -** ESL tools used to develop the hardware and software communications schemes for processor/memory designs
- **ESL Radio Frequency (RF) Design -** Behavioral and architectural tools used in frequency-based designs
- **Acceleration Libraries / Development Tools -** Libraries of hardware accelerators, for software functions, or the tools needed to develop the accelerators
- **Silicon Virtual Prototype -** A hardware virtualization platform that enables an RTL hand-off of a SoC

ESL VERIFICATION
Verification at the transaction level and above for hardware and software

- **Intelligent Test Bench** - The tool that partitions the design into verification blocks, assigns the necessary verification tool to the task, tracks verification coverage and, in general, automates the functional verification flow
- **ESL Formal Verification** - The process of mathematically proving that an ESL description equates to another ESL description or an RTL description (less specifically, that any design representation equates to another)
- **ESL Co-Verification** - Tool suites that include emulation, acceleration and simulation, starting at the ESL and continuing down into RTL design; used to verify hardware and software
- **Transaction-Based Acceleration & Emulation** – Acceleration and emulation using ESL transaction models as an input

ESL SOFTWARE DEVELOPMENT
Tools used for many-core/processing for parallel programming

- **Algorithm Design and Optimization** - Tools to assist system designers in the development of algorithms capable of parallel processing
- **ESL Compilation -** Parallel software compilers
- **Parallel Programming** - Tools for developing parallel programs
- **Many-core Development Tools** - Tools used to utilize and optimize the use of multicore, multiprocessor in systems
- **Software Virtual Prototype** - Virtualization tools used to allow the embedded software programmer to develop software prior to completed silicon
- **Model Development Tools** - Tools used to develop models for the Software Virtual Prototype
- **Algorithm Development & Optimization** - Tools used to develop Parallel algorithms or to optimize sequential algorithms for parallel computing
- **Network Simulation** - Tools used to simulate the performance of your web-based or telecommunications-based network

REGISTER TRANSFER LEVEL (RTL)

ACCELERATION/EMULATION Dedicated hardware/software tools that allow a designer to observe the function of a circuit prior to prototype.

RAPID PROTOTYPING Printed Circuit Boards used to speed up the verification of an SoC.

HARDWARE/SOFTWARE CO-VERIFICATION Tools for the simultaneous simulation and analysis of both the hardware and the software

RTL FUNCTIONAL VERIFICATION Tools and Verification IP used to assist simulation and Formal methods of verification

RTL DESIGN & ENTRY Tools to assist engineers in entering a design or analyzing the simulated results of that design. Includes use of graphical symbols to represent RTL VHDL or Verilog

RT LEVEL SIMULATION

- **Mixed-Signal Simulation** - Simulation which accepts both analog and digital inputs
- **Mixed-Language Simulation** - Simulation that can read both VHDL & Verilog, possibly also C/C++
- **Verilog** - Simulation using the Verilog Hardware Description Language
- **VHDL** - Simulation using VHSIC Hardware Description Language

RTL SYNTHESIS

- **Logic Synthesis** - Synthesis for gate array or cell-based design
- **FPGA Synthesis** - Synthesis for FPGA or CPLD design

PHYSICAL DESIGN ANALYSIS TOOLS

- **EMI Design** - Analysis of electromagnetic generation or interference for PCBs, ICs, cables connectors/packaging
- **Metal/Electromigration Design** - Unauthorized metal movement in an IC or PCB from excessive current density
- **Power Design** - Power consumption/distribution analysis
- **Signal Integrity Design** - Analysis of high-speed coupling effects (including transmission line and crosstalk) on signal lines and signal reflection/degradation on PCBs, MCMs, or ICs
- **Timing Design** - Verification of timing of a design; involves inputs to a physical circuit model simulation to test nondynamic functions of a design; static timing verification does not require test vectors to determine timing violations
- **Design Debug** – Tools used to track down coding errors and circuit failures in the design

DESIGN FOR TEST TOOLS

Tools used to determine, improve or add to the testability of electronic circuits

- **ATPG** - Automatic Test Pattern Generation tools
- **SCAN** - Test chain insertion
- **BIST** - Built-In Self Test tools; test structures placed in the design to allow the testing of silicon or PCB logic
- **Fault Simulation/Grading** - Tools that allow checking the percent of test coverage of a design

FORMAL ANALYSIS Formal methods for design verification

FORMAL VERIFICATION Mathematically proving an RT level description equates to a gate level description

DESIGN DEBUG Tools used to find coding errors in the Verilog or VHDL code

GATE LEVEL

SCHEMATIC CAPTURE A design process that consists of graphical schematic entry and netlist extraction

SIMULATION

- **Gate-Level** - Simulation based upon gate level netlist (not VHDL or Verilog)
- **Analog Simulation** - Simulation using only analog inputs

GATE-LEVEL DESIGN

- **RF Design & Simulation**- Frequency based design and simulation tools
- **Analog Design** - Tools used for the design and optimization of analog circuits
- **Gate/Transistor Level Design Tools** - Tools used to do circuit design at the lowest level of abstraction

MISCELLANEOUS

EDA ENTERPRISE AND COMPONENT INFORMATION SYSTEMS (CIS) TOOLS

Tools sold throughout the engineering organization to help train, document, and spread company-specific design practices; includes CIS libraries used in PCB design. Tools use for manage and optimize large server farms or the Cloud.

DESIGN LIBRARIES Description of elements used in EDA designs (i.e., components, simulation models, symbols)

INTEROPERABILITY TOOLS Database, tool management, library software including backplanes, file translators, and design environments

IC AND PCB/MCM/HYBRID CAD SUB-APPLICATION DEFINITIONS

IC LAYOUT

DRC Design rule and logic rule checkers used to perform final verification on an IC design prior to making masks

EXTRACTORS Tools used to determine the parasitic effects caused by the physical implementation

IC CAM

Computer-aided semiconductor manufacturing tools used to interface design with manufacturing for IC design

- **TCAD** - Technical CAD, semiconductor process development and monitoring tools
- **RET** - Resolution Enhancement Technology, includes Optical Proximity Correction (OPC)/phase shift and fracturing, is used to improve mask-making with technologies for the optical characteristics of lithography
- **DFY** - Tools designed to improve yield or to prevent catastrophic failure because of the effects of lithography or silicon variability

IC SPICE SIMULATION

SPICE or SPICE-like simulation using a derivative of the Berkeley SPICE transistor-level simulator

IC PHYSICAL ANALYSIS

Tools used to analyze the physical effects of the final layout of the design

- **EMI** - Analysis of electromagnetic generation and interference for ICs and cables/connectors packaging
- **Reliability and Metal/Electro Migration** - Analysis of current density and related issues that might cause the unauthorized movement of metal in an IC
- **Power** - Analysis of the power consumption of ICs and systems
- **Signal** - Analysis of high-speed coupling effects between signal line and reflection/degradation of high-speed signals on ICs, including transmission line and crosstalk analysis
- **Timing** - Verification of the timing of a design; the process usually involves providing inputs to a physical circuit model or computer simulation to test the non-dynamic functions of a design. Static timing verification does not require the use of test vectors to determine timing violations

IC PLACE & ROUTE

Tools used to transfer the design to a silicon mask generating format

- **ASIC Layout** - Tools used for gate array and CBIC layout
- **Custom IC Layout** - Silicon design tools that work at the transistor level. Also includes layout editors and process migration tools

PHYSICAL LIBRARIES & TOOLS

- **Physical Libraries** - Libraries that are directly tied to the physical layout of silicon
- **Library Development Tools** - Tools to automate the design of library models

3D IC

- **3D IC Simulation** - Tools capable of three dimentional simulation
- **3D Pathfinding** - Tools that enable three dimentional what-if analysis
- **3D Floorplanner** – Floorplanning in three dimentions
- **3D IC Analysis** – 3D Physical Analysis tools for Timing, Signal Integrity, EMI, Power, Thermal and Reliability

PCB LAYOUT

PCB LAYOUT

Tools used to design, place, and route a printed circuit board

MCM AND HYBRID DESIGN

Tools used to design, place, and route a multichip module or hybrid substrate

PACKAGE DESIGN

Software tools and solutions for the co-design of complex package physical design, analysis analysis of timing, power and signal integrity in IC packages and printed circuit boards

PCB VIRTUAL PROTOTYPE

Tools that use a virtual representation of the PCB to estimate physical effects up to the CAE level of the design

PCB CAM

Computer-aided manufacturing tools used to interface design with manufacturing for PCB design

PCB SPICE SIMULATION

SPICE or SPICE-like simulation using a derivative of the Berkeley SPICE transistor-level simulator

PCB PHYSICAL ANALYSIS TOOLS

Tools used to analyze the physical effects of the final layout of the design

- **EMI** - Analysis of electromagnetic generation and interference for PCBs and cables/connectors packaging
- **Power** - Analysis of the power consumption of PCBs, multichip modules (MCMs) and systems
- **Signal Integrity** - Analysis of high-speed coupling effects between signal line and reflection degradation of high-speed signals on PCBs or MCMs
- **Thermal** - Analysis of heat distribution in PCBs, multichip modules (MCMs) and systems
- **Timing** - Verification of the timing of a design; the process usually involves providing inputs to a physical circuit model or computer simulation to test the nondynamic functions of a design. Static timing verification does not require the use of test vectors to determine timing violations.