

The **2006 International Conference on Computer Aided Design (ICCAD)** featured a panel session **"CAD Research: Pay Now or Pay Later"**. The panel presenters were tasked with addressing various issues about the CAD EDA industry. Some of the most important issues, that bear repeating include:

- What are the top five CAD research challenges in the next five years?
- How will the EDA industry address these challenges?
- Where or how will these challenges be attacked with the most success?

According to various panel experts, yearly venture capital investment in the semiconductor industry reaches an **estimated \$10 billion**. CAD EDA captures about \$1 billion of that investment total annually. Panelist statements were wide and varied, but many key points are worth noting.

- Chip designs have become large, complex, and expensive
- Companies are shifting value to IP development
- More designs include non-digital devices. RF and mixed signal content could double by 2007
- New usable tools will be challenging and expensive
- SIP, SOC, flip chip and next generation wafer level CSP package designs will proliferate in 65nm and 45nm designs

According to some panelists, current EDA tools are efficient, but there is also "too much garbage" seeping into the industry because too many investors don't understand EDA or the EDA engineering skills needed to meet emerging complex designs at the chip and system level. The EDA industry can address some of these top challenges by

- Encouraging entrepreneurs and investors to do more and better homework on the EDA industry, a company's tools and qualifications
- Developing an EDA research center (similar to Sematech and SRC) supported by outside funding, company and university research consortia
- Investing in more time and training of the VC community

While all panelists agreed that the cost of addressing these challenges would be high, and that inefficiencies and redundancies still exist, the groups or people that could address and successfully attack these challenges would include

- The EDA industry that could support an R&D customer center that focuses on the future of EDA growth
- EDA industry vendors that worked more closely with University level research to guarantee that future EDA design engineers graduate with high quality EDA software skills
- The large EDA industry vendors that could develop and promote the right technology transfer model for funding EDA startups

Recent major technology shifts at the silicon, device, package and test levels that will drive more challenges but also CAD EDA design opportunities at the chip, package, PCB and system level include

- Clock multiplication- high end microprocessor clocks multiply input rate
- High-speed I/O's use local clocking (embedded clocks)
- Mixed-signal device and IP cores
- Multiple time domains (Asynchronous data transfers confound synchronous test processes)
- Redundancy and Repairable Circuits
- Tunable circuits (analog floating gates modify/optimize circuit behaviors)

The survivability of Moore's Law continues to be challenged. The latest prediction for Moore's Law to hit the brick wall of physics is 2025. The industry driving scaling and complexity challenges also contributes to its extension with new materials, new architectures and new innovations. The CAD EDA industry may play an even more important role not only by meeting the growing list of challenges. If it decides to pick up the gauntlet, the EDA industry could change the history of Moore's Law.

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