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EDA Tool User's Definitions

General Definitions

ASIC – Application Specific Integrated Circuit, generally a single customer IC, a design methodology

ASSP – Application Specific Standard Product, a multi-customer IC using the ASIC design methodology

EDA – Electronic Design Automation, tools used to develop ICs and electronic systems

CAE – Computer Aided Engineering (Electronic in this case)

CBIC – Cell-based IC, an ASIC where the entire design is placed in the silicon during the manufacturing process

CPLD – Complex Programming Logic Devices, similar to an FPGA but using a Complex Logic Block instead of gates. Like the FPGA they are manufactured and sold, then programmed by designer

FPGA – Field Programmable Gate Array – A standard product hard wired programmed by the User

Gate Array – An ASIC with rows of pre-manufactured gates that the designer can connect, using the top layers of metal, during the IC manufacturing process

IC – Integrated Circuit, Standard Product ICs

IC Layout – The act of developing and verify the files needed to produce a mask set for the manufacturing of semiconductors

PCB – Printed Circuit Board, an electrically connected board in which ICs, passive components and other semiconductors are mounted to form a circuit

PCB Layout – The act of developing and verifying the files needed to manufacture Printed Circuit Boards

SoC – System on Chip, a high gate count IC that includes at least one software programmable function

ESL Pyramid

SoC System Designer – An Engineer designing both the hardware and the software for a SoC IC

Board System Designer – An Engineer who is designing a PCB, including the software, that is a system or sub-system, which includes at least one software programmable function

Embedded System Software – An Embedded Software Engineer that develops software, for a dedicated, rather than general purpose, system

Semiconductor and PCB/FPGA Pyramid

Power User – An engineer that pushes the state-of-the-art. He/she works in teams that include a CAD group that develops In-House design tools. He/she usually uses an ASIC instead of an FPGA. He/she uses the latest Semiconductor silicon node. He/she is generally pushing the speed, power or complexity aspects of a design. The performance or cost of the ASIC/ASSP is the main completive advantage. High speed or large a number of board layers are common.

Upper Mainstream – An engineer that follows the Power User by one or two silicon nodes. He/she works with a CAD group that generally does not produce In-House tools. The design is an important part of the company's product, however high performance is not a necessity. The PCB designs are usually complex, although not necessarily high speed.

Lower Mainstream – An engineer that generally uses FPGAs for his designs, only using an ASIC when lower cost or higher performance is required. They have no CAD group support. The company's competitive advantage is not the electronic content of the product. Board design is often outsourced.

Late Adopter – An engineer that does low-end designs using low-cost EDA tools, either standard ICs or low-complexity FPGAs and, if an ASIC is required, lagging silicon nodes. Also in this category are high end, usually Analog or RF, designers using primarily discrete semiconductors and low-complexity standard ICs. Few EDA tools are needed. Boards are generally simple, produced with low cost tools.