

## THE EDP CONFERENCE...WORKSHOP...WHATEVER...

Some IEEE Conferences are hard to categorize; EDP and CANDE come to mind. EDP certainly isn't a show; there are no booths or entertainment. It isn't a workshop where someone comes in and trains the audience on a particular tool. It's more or less a working session; where presenters come in and present their ideas, not necessarily their conclusions, and then let the audience critique their approach. This makes for a rambunctious program that comes to grips with many of the problems in electronic design today. This is a Methodologist's Conference and marketing speak is frowned on.

## WHAT COMES AFTER CMOS?

A few of us use EDP to prepare for our work on the ITRS TWIGs (Technical Working Groups). One of my hot buttons has been the fact that the Roadmap now extends beyond 2020. And 2020 is the year CMOS is probably going to go off the rails. It's really difficult for us to come up with future design methodologies and future design tools if we don't know what we are designing.

Now CMOS is certainly not going to go away; after all Bipolar Semiconductors didn't go away when CMOS took off. CMOS is just no longer going to be the driver for Moore's Law. Some other technology will come to the forefront in electronic design. DARPA has a program that is exploring four possible approaches that may replace CMOS. Spintronics seems to be the leading candidate so far. EDP is the obvious Conference to explore these four approaches and we hope to put a session together next year to do just that.

## 3D-ICS

One of today's hot topics is 3D-ICs. We've been playing with the technology for a few years now with the stakeholders loudly proclaiming that it is the technology of the future. Most non-stakeholders can see a few memory intensive applications, some of which are in production today, but outside of a few killer apps they don't see a general use for the technology. The cost of building an infrastructure and the cost of manufacturing will keep it from moving to the mainstream.

Prior to EDP 2010 that was my view also. I felt that the main application would be concurrent memory, whenever we figure out how to design one, that will sit on top of many-core SoCs using TSVs (Through Silicon Vias) to minimize latencies. I'm not so sure today. CMOS was considered a niche process, primarily because of its relatively slow speed and high cost of manufacturing. If you look at breakthrough technologies one of the attributes is that it has actually been around long enough to get the major problems solved. With CMOS all it took was a few volume applications to shake out the rest of the bugs and it was off and running. Keep in mind that 2020 is not that far away and as we sit today 3D-ICs are the only technology that has any significant manufacturing experience of the new approaches. We'll have to wait and see what EDP 2011 brings but I have gained a new respect for 3D-ICs.