

## BACKGROUND

Ok, so maybe I'm exaggerating, but it was certainly the first one I've seen and I've seen a lot. For a little background I was part of the semicustom, or gate array community during the 1980s. When FPFAs hit the scene, in the mid 1980s, I took a look at them and easily come up with a formula that divided the gate array market from the FPGA market. It was based on production cost of the die and packaging. There was really not much conflict; FPGAs took up the low gate count end of the market, one that we were happy to relinquish due to low profit. At every node change FPGAs were capable of doing a higher percentage of the design starts, but the volume market was still a gate array, or standard cell ball game.

Towards the late 1980s the FPGA marketing establishment became dissatisfied with their fairly predictable market share and started exaggerating their capabilities. One of the ways they did this was by using what became known as the Paterson Gate. To get a Paterson gate count you took the number of ASIC gates that an FPGA could handle and multiply by four, or six if you were pushing performance. Other exaggerated claims were made and they were made loud enough and often enough to cause confusion in the market place.

In 1989 Stan Baker, of EE Times, put together a panel consisting of the marketing managers of the major FPGA vendors and me. The FPGA guys would give their pitch and then I would point out the exaggerations and sometimes outright lies, to the audience. The panel became popular and Stan shopped it around to most of the conferences. I don't think any of this did anything to move the market share needle, but it was all good fun. Unfortunately I got tagged as being anti-FPGA, which wasn't true.

## MOSHE TAKES OVER AS CEO OF XILINX

I've known Moshe for a while now and consider him a good friend. I've always known him to be honest, but even so moving to Xilinx he was bound to be influenced by the Xilinx culture. So I was interested how he was going to handle his presentation at SNUG. He didn't let me down, and as the title of this note says I heard my first honest FPGA presentation.

## THE NEW FPGA MARKET

Not to take any credit away from Moshe, it was actually not difficult to put an end to the exaggerated marketing claims of the past. The reason is that at 45nm an FPGA had enough gates to do true SoC designs. That has opened up a whole new world to the FPFAs designer. Now will that bring an end to the ASIC market as we know it? Of course not and Moshe made a point of saying so. What has happened though is a convergence of enough gates, true globalization of electronic design and the move to ES design and you have the reverse of the perfect storm. Everything has become bright and shiny for the FPGA world. Moshe's move to Xilinx couldn't have come at a better time. His experience in both the ASIC business and the EDA business added to his mature, level headed management style is just what the FPGA world needed to take advantage of this golden opportunity. Xilinx is in for quite a ride.